WHAT IS CLAIMED IS:

1. A synchronous transport module (STM), comprising:

a universal test, operation, and physical interface for asynchronous transport mode (UTOPIA) interface that transmits UTOPIA level-2 data;

a pair of STM interfaces that receive UTOPIA level-1 data;

a UTOPIA memory that converts the UTOPIA level-2 data into the UTOPIA level-1 data and transfers the UTOPIA level-1 data to the pair of STM interfaces, according to a transmission address; and

a UTOPIA interface control part that converts the transmission address, depending on states of the pair of STM interfaces.

2. The STM of claim 1, wherein the UTOPIA memory is a first in first out (FIFO) memory.

3. The STM of claim 1, wherein the UTOPIA interface control part assigns one of the pair of STM interfaces, having a failure, to a standby state and another of the pair of STM interfaces, not having a failure, to an active state.

4. The STM of claim 3, wherein the transmission address is converted by inverting a value of a least significant bit in the transmission address.

5. A synchronous transport module (STM), comprising:

a universal test, operation, and physical interface for asynchronous transport mode (UTOPIA) interface that communicates UTOPIA level-2 data;

a pair of STM interfaces that communicate UTOPIA level-1 data;

a UTOPIA memory that converts the UTOPIA level-2 data into the UTOPIA level-1 data and transfers the UTOPIA level-1 data to the pair of STM interfaces, according to a transmission address;

a first bus-matching memory that converts the UTOPIA level-1 data from a first STM interface, of the pair of STM interfaces, into the UTOPIA level-2 data and transfers the converted UTOPIA level-2 data to the UTOPIA interface, according to a reception address;

a second bus-matching memory that converts the UTOPIA level-1 data from a second STM interface chip, of the pair of STM interfaces, into the UTOPIA level-2 data and transfers the converted UTOPIA level-2 data to the UTOPIA interface chip, according to the reception address;

a processor that reads states of the pair of STM interfaces; and

a UTOPIA interface control part that converts the transmission address and the reception address, under the control of the processor.

6. The STM of claim 5, wherein the UTOPIA interface control part assigns one of the pair of STM interfaces, having a failure, to a standby state and another of the pair of STM interfaces, not having a failure, to an active state.

7. The STM of claim 5, wherein the processor is a programmable logic device (PLD).

8. The STM of claim 5, wherein the UTOPIA memory, the first bus-matching memory, and the second bus-matching memory are first in first out (FIFO) memories.

9. The STM of claim 5, wherein the UTOPIA interface control part stores first bits, used to determine whether each of the pair of STM interfaces is assigned a duplex state or a simplex state, and second bits, used to determine whether each of the pair of STM interfaces assigned the duplex state is further assigned an active state or a standby state.

10. A method for transmitting data in a synchronous transport module (STM), including a universal test, operation, and physical interface for asynchronous transport mode (UTOPIA) interface for transmitting UTOPIA level-2 data, a pair of STM interfaces for receiving UTOPIA level-1 data, a UTOPIA memory for converting the UTOPIA level-2 data into the UTOPIA level-1 data and transferring the UTOPIA level-1 data to one of the pair of STM interfaces, according to a transmission address, and a processor, the method comprising:

(a) checking a fail state of each of the pair of STM interfaces with the processor;

(b) assigning one of the pair of STM interfaces, having the fail state, to a standby state and another of the pair of STM interfaces, not having the fail state, to an active state;

(c) converting the transmission address in accordance with the fail states of the pair of STM interfaces; and

(d) transmitting the converted UTOPIA level-1 data to the STM interface having the active state, according to the transmission address.

11. The method of claim 10, wherein the processor is a programmable logic device (PLD).

12. The method of claim 10, wherein the transmission address is converted by inverting a value of a least significant bit in the transmission address.

13. A synchronous transport module (STM), comprising:

a plurality of STM interfaces that communicate universal test, operation, and physical interface for asynchronous transport mode (UTOPIA) level-1 data;

a UTOPIA interface control part that communicates UTOPIA level-2 data and assigns an operational state and a communication mode to each of the plurality of STM interfaces; and

a plurality of bus-matching first in first out (FIFO) memories that communicate the UTOPIA level-1 data with the plurality of STM interfaces and the UTOPIA level-2 data with the UTOPIA interface control part, convert the UTOPIA level-1 data to the UTOPIA level-2 data, and convert the UTOPIA level-2 data to the UTOPIA level-1 data, wherein

each of the plurality of bus-matching FIFO memories corresponds to a separate one of the plurality of STM interfaces and communicates UTOPIA level-1 data with only the corresponding STM interface.

14. The STM of claim 13, wherein the UTOPIA interface control part assigns each of the plurality of STM interfaces to operate in a duplex mode or a simplex mode, for the respective communication mode, and assigns each of the plurality of STM interfaces the operational state of active state or standby state, based on an operational status of the respective STM interface.

15. The STM of claim 14, wherein:

each of the STM interfaces assigned the duplex mode of operation is paired with another STM interface and only one STM interface of each pair is assigned the active state; and

only the active state STM interface, of each pair of STM interfaces, communicates with the UTOPIA interface control part.

16. The STM of claim 14, wherein each of the plurality of STM interfaces experiencing a detectable fault is assigned the standby state.

17. The STM of claim 15, wherein the UTOPIA interface control part changes a portion of a destination address of the UTOPIA level-2 data to uniquely identify the one STM interface, of a particular pair of duplex mode STM interfaces that are both partially addressed by the destination address, that is currently assigned the active state.

18. A synchronous transport module (STM) communication method, comprising:

communicating universal test, operation, and physical interface for asynchronous transport mode (UTOPIA) level-1 data between a plurality of STM interfaces and a plurality of bus-matching first in first out (FIFO) memories;

communicating UTOPIA level-2 data between a UTOPIA interface control part and the plurality of bus-matching FIFO memories; and

converting the UTOPIA level-1 data, received by the plurality of bus-matching FIFO memories, to the UTOPIA level-2 data and converting the UTOPIA level-2 data, received by the plurality of bus-matching FIFO memories, to the UTOPIA level-1 data, wherein

each of the plurality of bus-matching FIFO memories corresponds to a separate one of the plurality of STM interfaces and communicates UTOPIA level-1 data with only the corresponding STM interface.

19. The method of claim 18, further comprising:

assigning each of the plurality of STM interfaces to operate in a duplex mode or a simplex mode of communication; and

assigning each of the plurality of STM interfaces an operational state of active state or standby state, based on an operational status of the respective STM interface.

20. The method of claim 19, further comprising:

pairing each of the STM interfaces assigned the duplex mode of operation with another STM interface, wherein

only one STM interface of each pair is assigned the active state, and

only the active state STM interface, of each pair of STM interfaces, communicates with the UTOPIA interface control part.

21. The method of claim 19, further comprising assigning each of the plurality of STM interfaces experiencing a detectable fault the standby state.

22. The method of claim 20, further comprising changing a portion of a destination address of the UTOPIA level-2 data to uniquely identify the one STM interface, of a particular pair of duplex mode STM interfaces that are both partially addressed by the destination address, that is currently assigned the active state.